

DiaSys: On-Chip Trace Analysis for Multi-Processor System-on-Chip

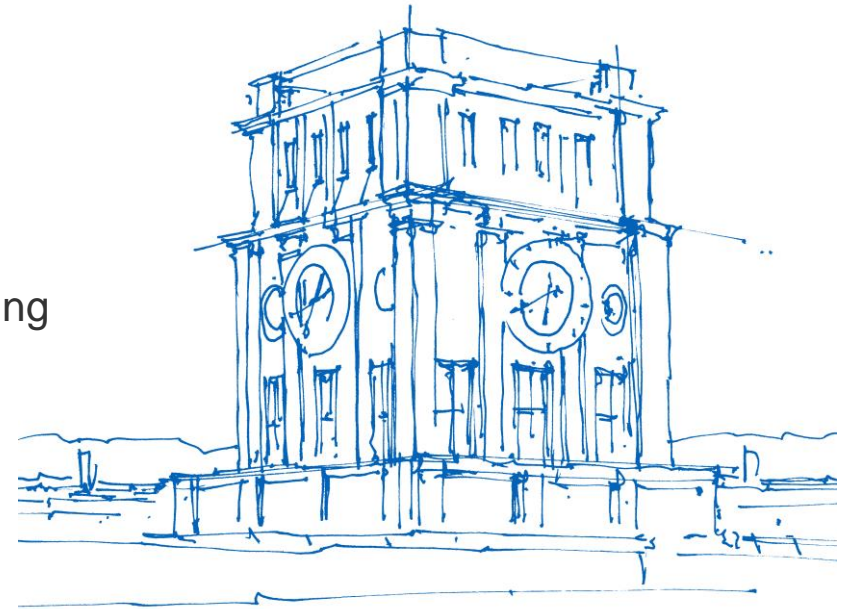
Philipp Wagner, Thomas Wild, and Andreas Herkersdorf

Technical University of Munich

Department of Electrical and Computer Engineering

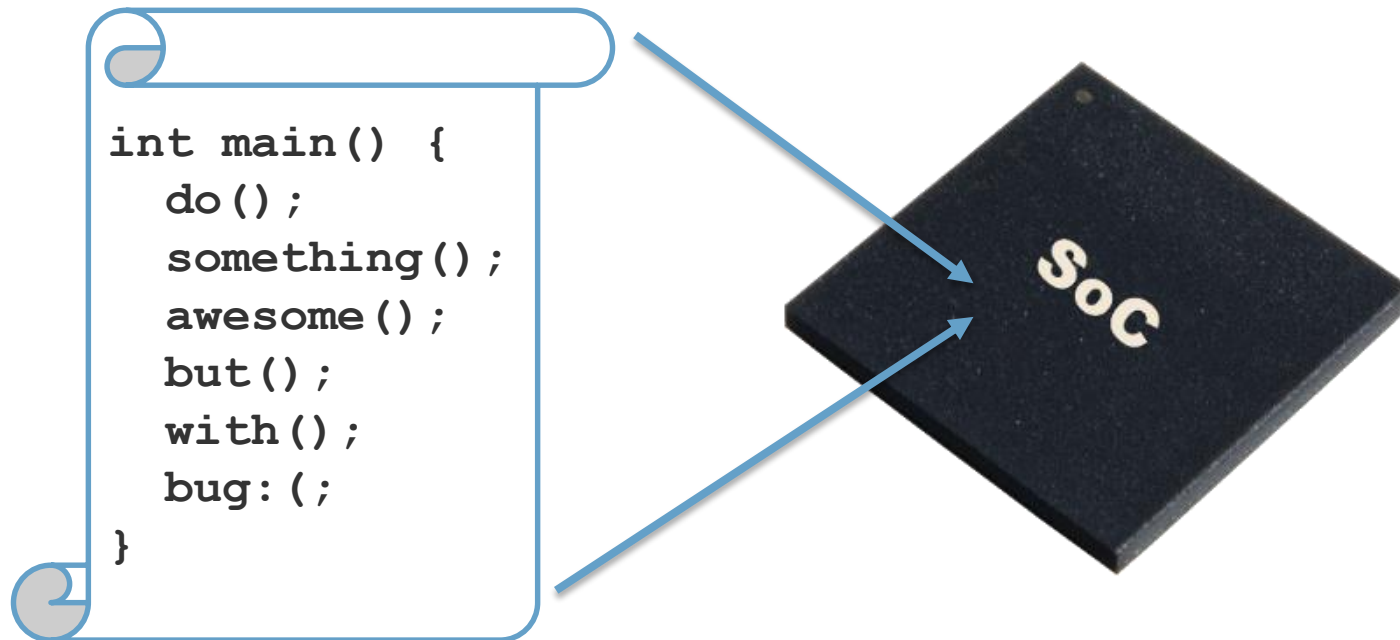
Institute for Integrated Systems

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Uhrenturm der TUM

Software Debugging on a SoC



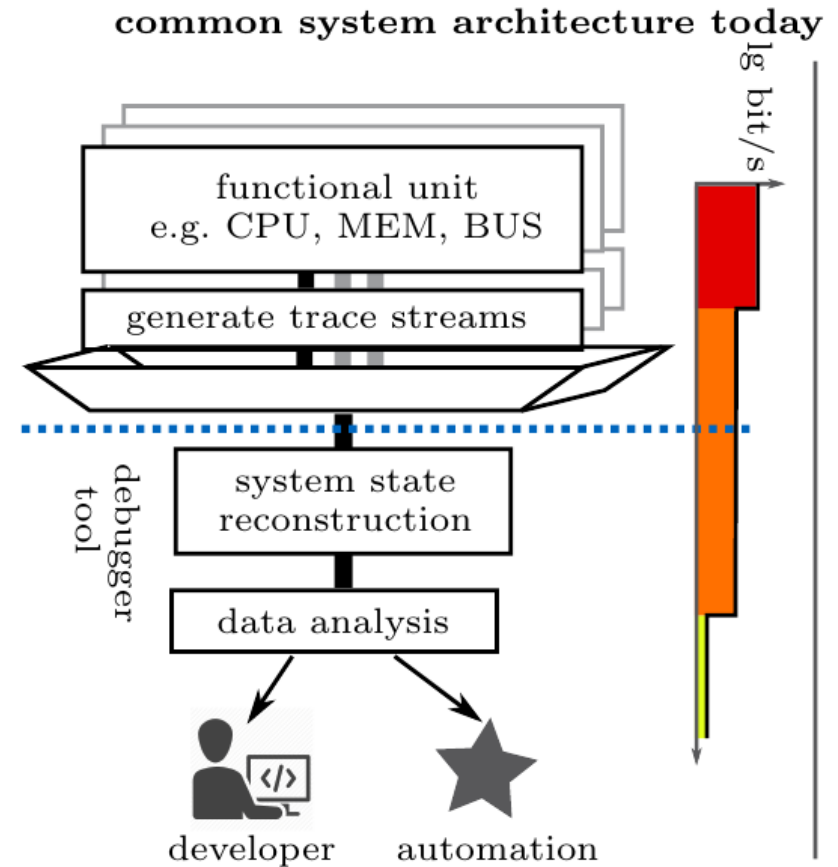
Run-control
debugging

vs.

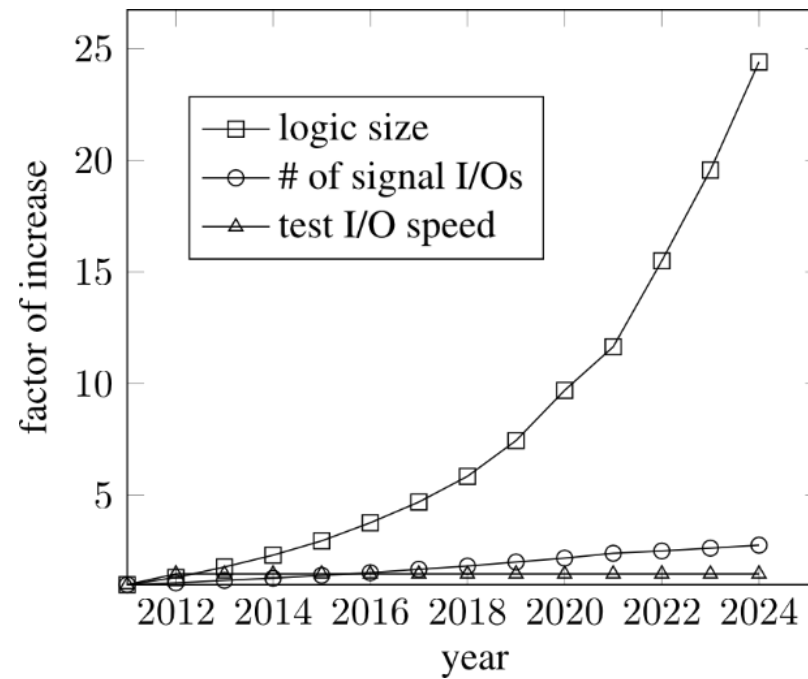
tracing

Tracing Today

- ARM CoreSight
- NEXUS 5001
- Infineon MCDS

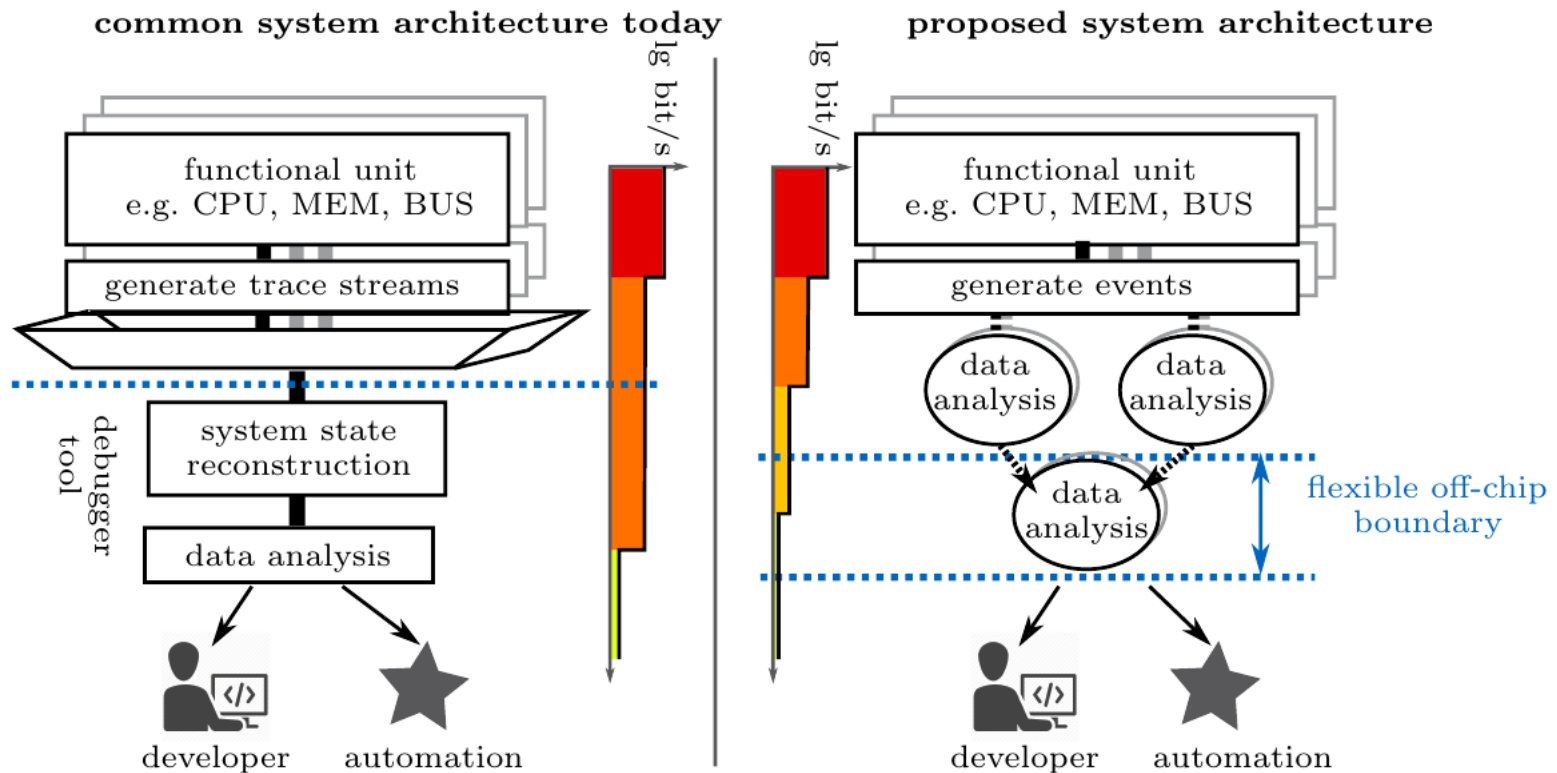


Future Proof?



Data from ITRS roadmap, 2013 edition.

DiaSys: On-Chip Trace Analysis



DiaSys: Event-Based Diagnosis



Events

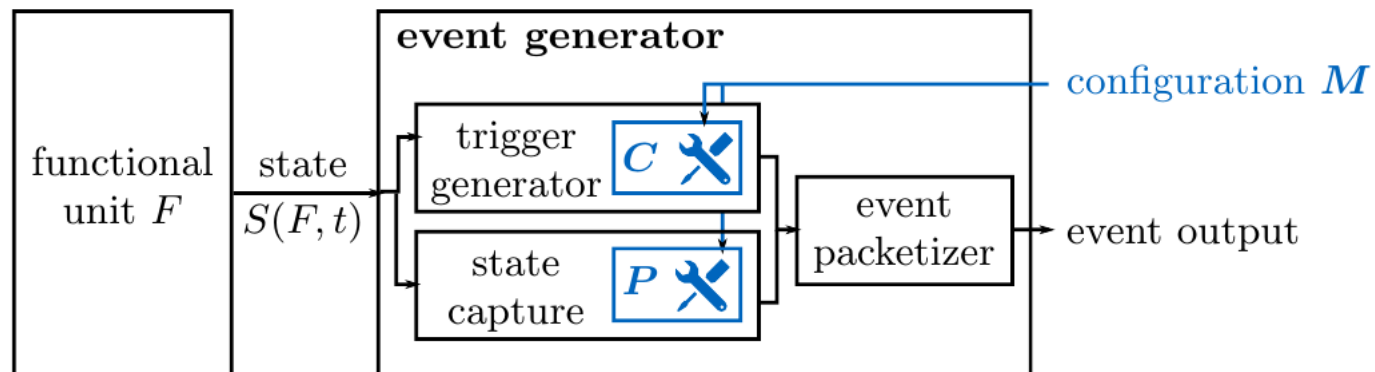
The Information Container

- Event Type
 - uniquely identify the type of the event
- Timestamp
 - Ordering
 - Correlation
- Event Data
 - data associated with the event
 - usually synchronous with the event

Event Generators

... generate events

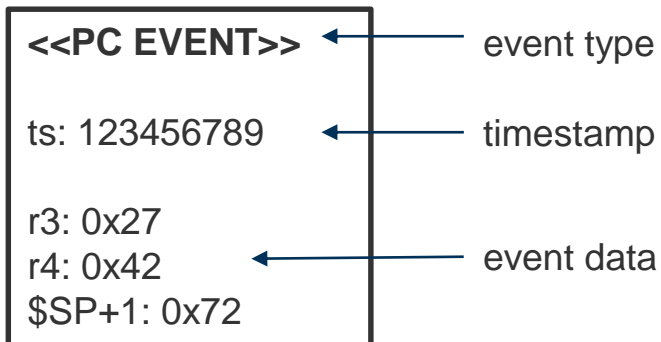
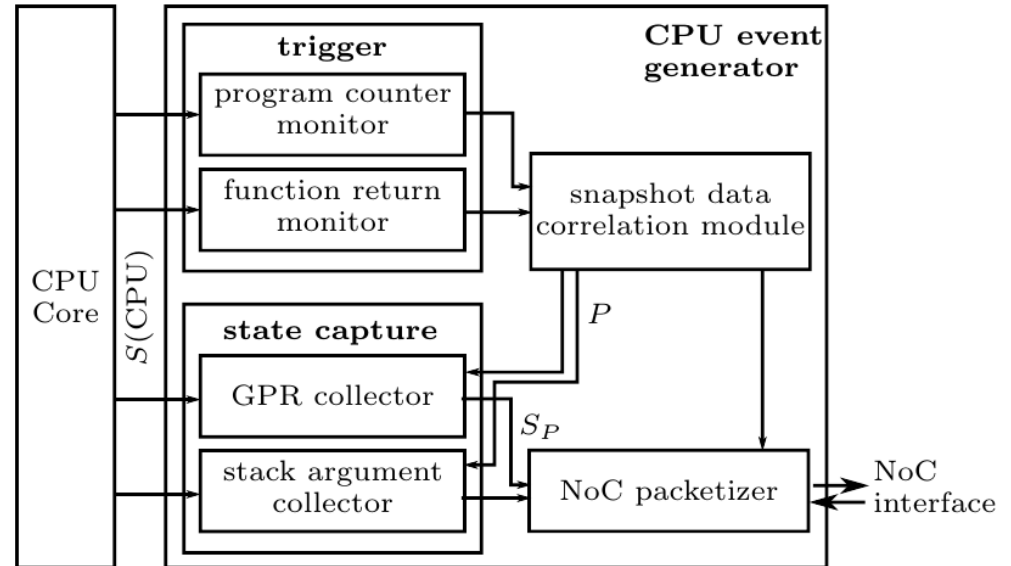
- observe the functional system
- (in general) configurable
 - triggers
 - event data (“payload”)
- configuration and NoC interface conforming to a common interface
- “synchronous island”



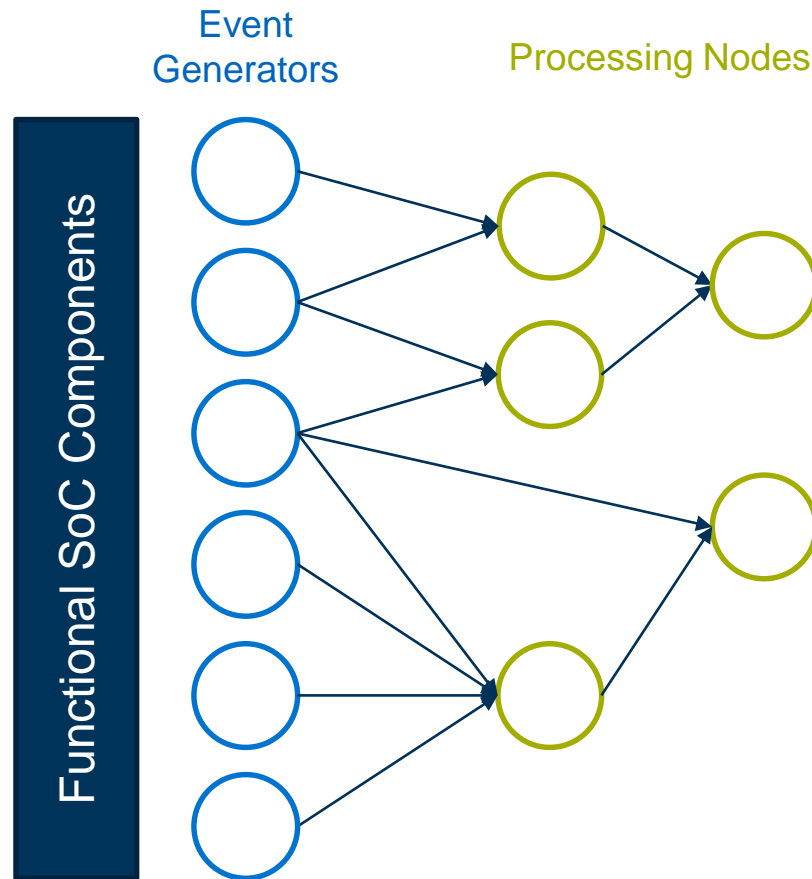
Core Event Generator

Event Generator for CPUs

- Triggers
 - PC (+ special cases)
- event data (sync)
 - register values
 - stack arguments



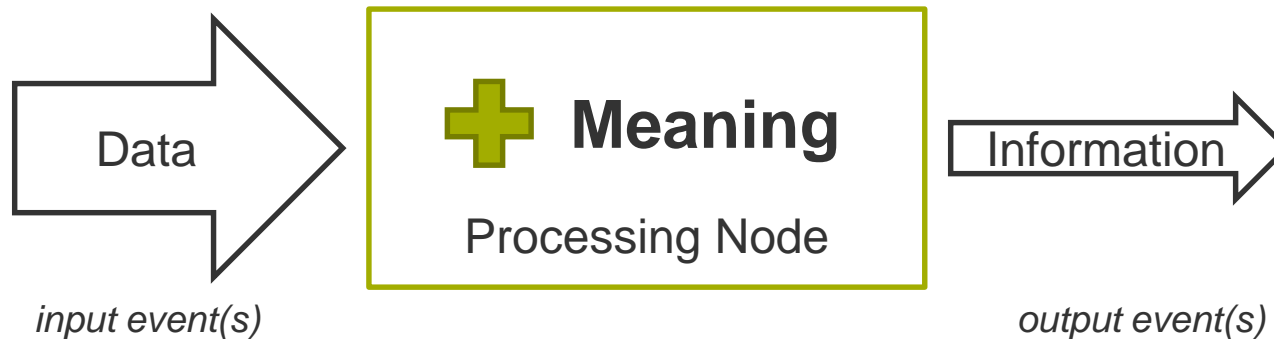
DiaSys: Event-Based Diagnosis



Processing Nodes

... transform events

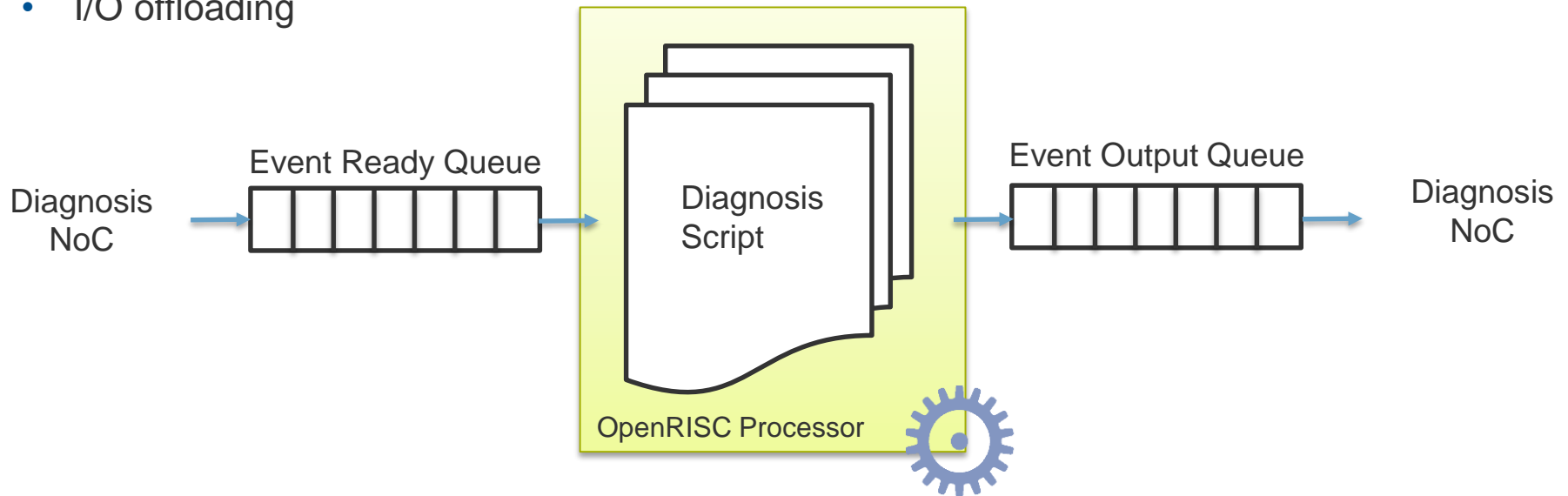
- Less data, more information
- Combine, filter, average, ...



Diagnosis Processor

A Programmable Processing Node

- full-featured 32 bit RISC ISA with FPU
- low overhead run-to-completion processing
- interrupt-free hardware scheduler
- I/O offloading



DiaSys: Architecture View

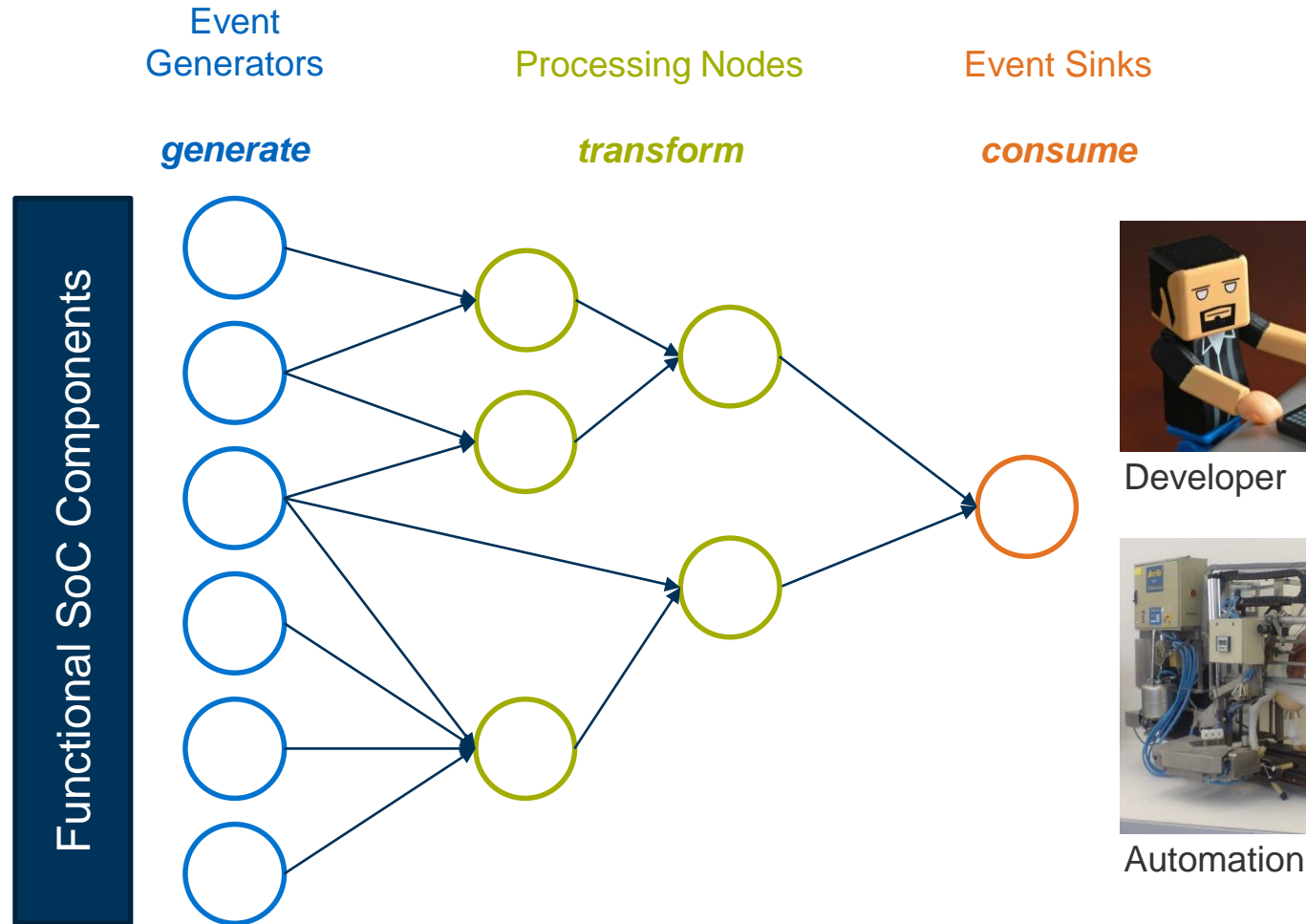
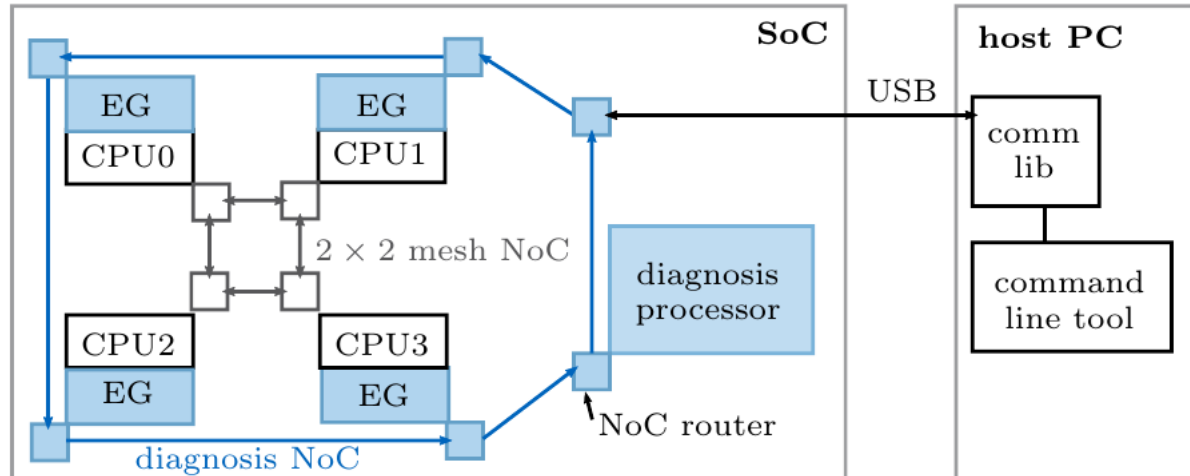


Photo: herval on flickr, CC BY 2.0

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Prototype Implementation: System View



Resource Usage

Module	LUTS	REGS	RAMS
functional system	40625	29638	80
1 compute tile (system contains 4)	~ 7232	~ 4763	20
2 × 2 mesh NoC	10791	9964	0
support infrastructure (DRAM if, clock/reset mgr)	904	623	0
diagnosis system	19556	19140	147
1 CPU Event Generator	3603	6521	2
1 CPU Event Generator (CoreSight-like functionality)	1365	1594	0
1 Diagnosis Processor	8614	4549	145
diagnosis NoC	2520	2926	0

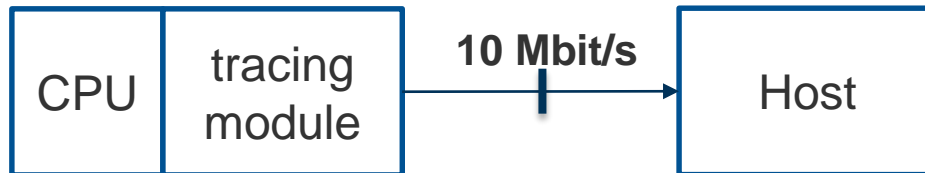
Results for a ZTEX 1.15d board with a Xilinx Spartan-6 XC6SLX150 FPGA. Synthesis results by Synplify Premier.

Usage Example

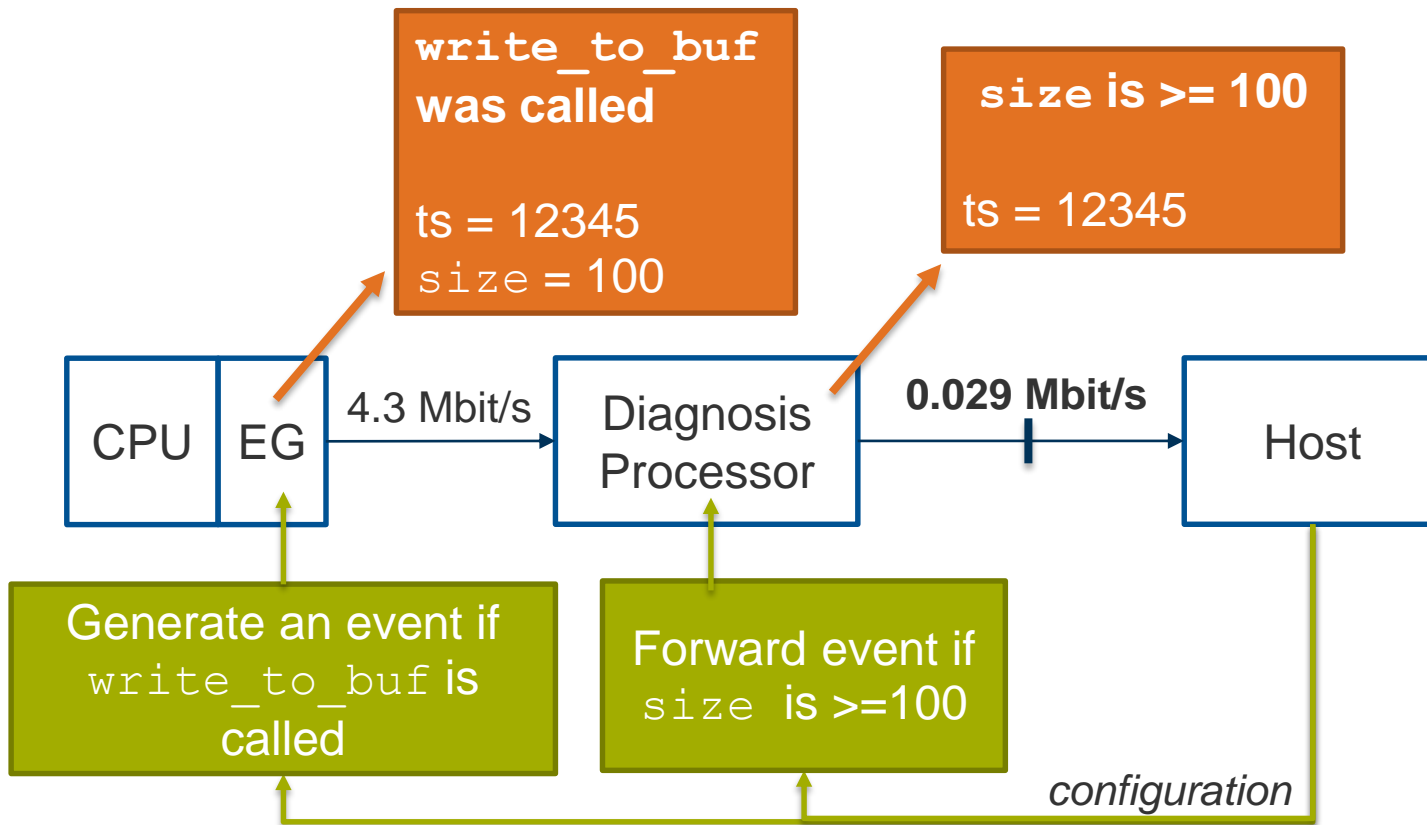
```
1 void write_to_buf(char* string, uint32_t size) {
2     struct {
3         char buf[99];
4         char var;
5     } test;
6     /* ... */
7     strncpy(test.buf, string, size);
8     /* ... */
9 }
10
11 int main(int argc, char** argv) {
12     char teststr[100] = "string_100_chars_long...";
13     for (int i = 0; i < 10000000; i++) {
14         uint32_t len = (i % 100) + 1; /* len [1;100] */
15         write_to_buf(teststr, len);
16     }
17     return 0;
18 }
```

Usage Example

- Setup: Example running on one 25 MHz CPU with IPC = 0.2
- Traditional tracing (CoreSight ETM, NEXUS 5001 Class 3)
(numbers scaled to our prototype implementation)
 - Full system trace (compressed to 2 bit/instruction)
 - data trace of writes to `size` (uncompressed)



Usage Example



one event if `write_to_buf` is called (event packet size: 12 byte);
 every 100th CPU event generates an off-chip event (event packet size: 8 byte)

Summary

We propose:

- Use self-contained **trace events**
- to enable **on-chip trace processing**
- to overcome the trace off-chip bottleneck.

Outlook

- System dimensioning for specific bug types
- Knowledge formulation
 - Adapt knowledge to specific system instance

Thank you! Questions?

Author contact

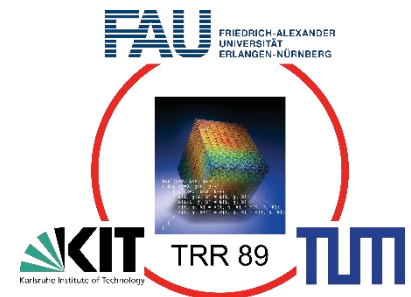
Philipp Wagner
Institute for Integrated Systems, Technical University of Munich
Arcisstr. 21, 80333 München, Germany
philipp.wagner@tum.de

Paper reference

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Backup Slides

Implementation: Diagnosis Processor

